REMARKS/ARGUMENTS

Reconsideration and allowance are respectfully requested. No new matter has been added by the amendments herein.

Claim Objection

Claims 3 and 4 are objected to for depending from "claims 1 or 2" even though claim 2 has been canceled. Claim 3 is amended to depend only from claim 1, and so it is believed that this objection is overcome

Claim Rejections

Claims 1, 3-9, and 11-15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,781,799 to Leger, et al. ("Leger") in view of U.S. publication no. 2003/0033454 A1 to Walker et al. ("Walker"). Applicant respectfully traverses this rejection.

Independent Claim 1

Independent claim 1 recites associating with output buffers and input buffers of DMA modules coupled in a chain, at least one intermediate block to control data transfer between the coupled buffers. The Office Action compares the recited DMA modules with DMA controllers 20 of Leger (Fig. 2), and the recited intermediate block with descriptor queue 24 of Leger (Fig. 2). And, because the Office Action is comparing descriptor queue 24 with the recited intermediate block, it appears that the Office Action must be comparing the recited buffers with common buffer pool 28 of Leger (Fig. 2).

However, Leger fails to teach or suggest transferring data between the buffers 28. Leger discloses that a given DMA controller 20 may store or retrieve data into or out of one or more of the buffers 28 for transfer to/from the host computer. Leger, col. 2, lines 27-30; Fig. 2. But there is no transfer *between* those buffers 28.

Moreover, descriptor queue 24 does not control data transfer of any kind, and thus cannot be properly compared with the recited intermediate block. Descriptor queue 24 is simply a storage element that stores the starting address of each of the buffers in common buffer pool 28, so that DMA controllers 20 know where to find each selected buffer. Leger, col. 4, lines 34-35;

col. 5, lines 44-49. In fact, descriptor queue 24 merely functions as a passive address book. If anything in Leger is controlling data transfer, it certainly cannot be descriptor queue 24.

The Office Action goes on to argue that it would have been obvious to modify Leger to incorporate input and output buffers that are allegedly part of the multi-port DMA of Walker Fig. 2 into each of the DMA controllers 20 of Leger. If this is the case, then descriptor queue 24 of Leger, which stores buffer 28 addressing, certainly could not have any involvement in the operation of the those added input and output buffers in DMA controllers 20, and so for this additional reason could not be the recited intermediate block.

Moreover, the chain arrangement of Walker cannot be applied to the system of Leger to result in the claimed chain arrangement of DMA modules. Walker discloses a single multi-port DMA having four ports A, B, C, and D. Walker, Fig. 2. The alleged chain arrangement in Walker is due to the sixteen possible combinations for connectivity between ports A, B, C, and D of a single multi-port DMA controller (Walker, Fig. 2; Office Action, p. 5). Thus, even if each DMA controller 20 of Leger is modified to contain the multi-port DMA controller of Walker, the alleged chain arrangement of ports A, B, C, D in Walker still would not result in chaining between DMA controllers 20 of Leger, but rather between ports A, B, C, and D, internally within a given one of the DMA controllers 20 of Leger.

In fact, it is respectfully submitted that the Office Action is confusing the multi-port controller of Walker with the ports A, B, C, D of that multi-port controller. In particular, it appears that the main point of the rejection is to modify Leger by incorporating each of the DMA controllers 20 of Leger with its own multi-port controller of Walker (each including ports A, B, C, and D). But then the Office Action relies on features in Walker relevant only to communications *between ports A, B, C, and D of a given multi-port controller*, rather than communications between several multi-port controllers of Walker (e.g., see the discussion of port chaining on page 6 of the Office Action).

Reliance on this latter feature suggests that the rejection is flipping between an embodiment in which each DMA controller 20 of Leger contains an entire multi-port controller of Walker, and an embodiment in which each DMA controller 20 of Leger contains only a single port A, B, C, or D of the multi-port DMA controller of Walker. Thus, the end-to-end logic of the rejection does not hold together and does not make out a *prima facie* case of obviousness. And,

if in fact each DMA controller 20 of Leger only contains one or two ports of the multi-port controller of Walker, then there would be no ports remaining for each DMA controller to be associated with its own respective IP block as recited in claim 1.

Moreover, contrary to the Office Action's assertion on pp. 4-5, Walker does not teach or suggest that the multi-port controller has input and output buffers in the manner claimed. The Office Action specifically refers to the statement in Walker in paragraph 0004 that data is buffered by a DMA controller. However, this statement has nothing to do with the multi-port DMA controller embodiment having ports A, B, C, and D and relied upon by the Office Action elsewhere in the rejection. Rather, paragraph 0004 is discussing the background, i.e., a completely different embodiment. In other words, Walker does not teach or suggest an embodiment that contains input and output buffers and that also utilizes ports A, B, C, and D. While Walker does disclose that a FIFO buffer may be used between the multi-port DMA controller and the bus (Walker, paragraph 0038), this FIFO buffer is clearly not relied upon by the Office Action and is also not relevant to the proposed modification of Leger.

Accordingly, in addition to the above-discussed problems, it is not at all clear which buffer in the multi-port DMA controller of Walker is being relied on by the Office Action to be incorporated into Leger. Should the Examiner continue to assert this rejection, it is respectfully requested that the Examiner clarify for the record which buffers in Walker are being relied upon.

For at least these reasons, Leger and Walker, either alone or in combination, fails to teach or suggest the above-discussed features of claim 1.

Independent Claims 5 and 11

Independent claims 5 and 11 are also allowable over Leger and Walker for at least similar reasons as discussed above with regard to claim 1.

Dependent Claims

The dependent claims are also allowable by virtue of depending from allowable independent claims, and further in view of the additional features recited therein.

Conclusion

All rejections having been addressed, Applicant respectfully submit that the present application is in condition for allowance, and respectfully solicit prompt notification of the same. Should the Examiner have any questions, the Examiner is invited to contact the undersigned at the number below.

Respectfully submitted,

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